Analytical Models Synthesis of Power Electronic Converters

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Abstract—In this paper we propose a synthesis of different mathematical models of power electronic converters based on Thevenin/Norton equivalent circuits. Those models, composed by impedances and harmonic noise sources, are helpful to predict the conducted ElectroMagnetic Interferences (EMI) generated by converters connected to the electrical network. Moreover, the extracted impedances are determining for sizing EMC filters. The proposed analytical model is tested with PSpice simulations and validated by experimental measurements, from DC frequency until 30MHz.

Index Terms—EMC modeling, differential mode, common mode, EMC filter, LISN, EMI, conducted noise, noise source.

I. INTRODUCTION

Nowadays, modern networks -such as the car’s network supplying many electrical actuators- include many converters to manage efficiently the power transfer, which creates new issues and therefore the EMC study becomes more and more complex.

Generally, in modern embedded networks, integrated actuators are supplied by DC power, the reason that DC-converters are strongly needed, to manage the corresponding energy. For example, the input power at aeroplane turbine sides may be 10 times greater than at actuator sides. The velocity and position control need also the control of the input power.

In order to comply with ElectroMagnetic (EMC) standards, an accurate prediction of a common mode (CM) and differential mode (DM) conducted noise is necessary. Furthermore, since ElectroMagnetic Interference (EMI) filters are coupled to converters, the optimisation is necessary reached with the knowledge of converter’s impedances [1–3]. Several papers treat the converter’s modelling with different techniques: Terminated/Unterminated models [4–6], lumped circuits [7–10]...etc. However, the proposed models deal only with one kind of converter, this cannot be generalised to other conditions, due to the parameter’s dependency. This paper, presents a noise source analytical models of two converter’s topologies, in order to highlight the impact of some parameters in the spectrum model profile, and highlights factors which actually make difference between such or that models.

This paper is organised in five sections. Section II gives the analytical computing process of the model. Section III is the application of the model on two converter structures. In the section IV we expose the impact of some parameters on the impedance. The last section concludes this paper.

II. GENERAL PURPOSE

DC-converters under some operation conditions are Linear and Time Invariant Systems (LTI), as mentioned in [2]. Based on this affirmation, they may be modelled by an equivalent Norton/Thévenin circuit. Moreover, converters under study are checked for this characteristic as demonstrated on the Fig.1. For frequencies higher than some tens of kHz, the input impedance is the same whatever the switches states.

A. Converter impedances computing

The main purpose of this work is to make a study about DM converters’ impedances taking into account its global behavior, such as the switching operation and PCB imperfections, and then extract a general law about a propagating path of DM conducted noise, by making a comparison point.

Power converters, especially DC-converters are supplied by two wires “L” for “Plus” and “N” for “Minus”, but also connected to a third wire “G” which is the safety conductor commonly called “Ground” conductor, since the converter is the main source of conducted interferences, due to its operation principle. Thus, DC-converters may be considered as three ports systems, as drawn in the Fig.2 [11]. Where: $Z_{LG}$,
In the context of the study, connect the ground wire "G", Z_LG and Z_NG which are commonly supporting the CM current.

\[ Y_{DM} = Y_{LN} + \left( \frac{Y_{LG} + Y_{NG}}{4} \right) \]  

(2)

B. The context of the study

The main idea of this paper is to extract a reliable analytical model to compute the DM impedance of DC-converter topology, connected to an electrical network (Fig.3), on a frequency range from very low frequencies up to few tens of MHz.

The purpose in computing this impedance is multiple:
- To compute network impedance,
- To manage to make an EMC analysis of a whole network,
- To contribute on the EMI filter optimization,
- To enhance the converter design.

III. ANALYTICAL MODELLING

A. The switching function

Any input signal S_m(t) crossing throw any switching cell, as drawn in the Fig.4, is choppes according to the control law sw(t) of the switching cell. The system outputs may be expressed according to (3).

\[ S_{out}(t) = sw(t) \cdot S_m(t) \]  

(3)

The switching operator sw(t), which is a T_{sw}-periodical function, actually establishes the switching law of the converter’s devices and depends on the control strategy, which in this case concerns the buck and the boost converters’ control, considering the duty cycle “\( \alpha \)”. Since the function sw(t) corresponds to the switching signals, we can imagine that its shape in the temporal domain, is a “one” and “zero” sequence level as drawn in the Fig.5. According to the signal processing theory, the switching operator may be expressed as in (4), by the convolution between two conventional functions, [1-3] and [11]:

- \( \Pi_{\alpha T_{sw}/2} (t) \) is the window function,
- \( \Pi_{T_{sw}} (t) \) is the Dirac Comb,
- Where \( T_{sw}=F_{sw}^{-1} \)is the switching period.
- \( \alpha \) is the duty cycle,

\[ sw(t) = \left( \Pi_{\alpha T_{sw}/2} \left( t - \frac{\alpha T_{sw}}{2} \right) \right) \otimes \Pi_{T_{sw}} (t) \]  

(4)

In the frequency domain, and by developing the convolution product, the output signal S_{out}(f) (Fig.4) can be expressed as in (5), where F_{sw} is the switching frequency.

In fact, the S_{out}(f) signal may be the converter current or voltage chopped at F_{sw} frequency whose importance will be highlighted when developing the expression.

\[ S_{out}(f) = \alpha \sum_{k=-\infty}^{+\infty} \sin(\pi \alpha k) \cdot e^{-j 2 \pi \alpha k/2} \cdot S_{in}(f-kF_{sw}) \]  

(5)
IV. CONVERTERS UNDER STUDY

A. Converters’ topologies

The DC-DC converters under study are schematised on Fig.8 and Fig.9. All essential coupling paths are introduced in order to be more accurate as in experiment, such as parasitical capacitances to the ground \((C_{LG}, C_{NG}, \text{and } C_{m} \text{ for both the buck and the boost converter})\), parasitical line inductances \(l_p\), parasitical elements of the boost inductor \(C_f\) and imperfections of both capacitors \(C_f\) and \(C_o\). [10].

B. Systems identification

The identification, of different parameters of converters’ topologies, drawn in Fig.8 and Fig.9, is performed by the impedance analyser “Agilent 4294A”. The measurement setup is illustrated in Fig.10.
1) Capacitors’ model identification

The decoupling capacitor’s impedance $Z_{Cx}(C_x$ for $C_f$ or $C_o)$, is modelled by three serial elements: the capacitance “$C_x$”, the serial inductive element “esl”, and the serial resistive element “esr” as expressed in (9). Those elements are identified by the impedance analyser 4294A. Fig.11 shows the comparison between the model and the measured impedance.

$$Z_{Cx}(p) = \frac{1}{C_x \cdot p} + esl \cdot p + esr$$

(9)

Fig. 11. The input capacitor’s impedance: (red) the serial element model, (blue) the measured impedance.

2) Parasitical elements

Converters’ parasitical elements are identified by the impedance analyser 4294A. The parasitical elements such as, the line inductances $I_p$, the capacitances to the ground $C_{LG}$, $C_{NG}$ and $C_m$ are deduced from measured impedances of the Fig.12, depicted between the “$L$” (or “$N$”) and the “$G$” wire. The $C_m$ capacitance, between the heatsink and the ground, is estimated according to (10), which is the plane capacitor equation.

$$C_m = \varepsilon_0 \varepsilon_r \frac{s}{e}$$  

(10)

- $\varepsilon_0$ and $\varepsilon_r$ are respectively the permittivity of the air and the relative permittivity of the insulator mica ($\varepsilon_r=5$)
- $Z_{LG}$: impedance between Plus-Ground wires,
- $Z_{NG}$: impedance between Minus-Ground wires,

3) Boost inductor

The boost inductor is the essential element in the Boost converter structure, since it is one which controls the variation of the current (state variable). Hence, its impedance is not without effect on the global DM impedance of the converter. Moreover, the equivalent HF model given in the Fig.13 is composed by a parallel resistive element “epr” and a parallel capacitive element “ecp”.

Fig. 13. The equivalent model of the boost inductor $Z_{boost}$

Fig.14 is the boost inductor impedance measured by the impedance analyser Agilent 4294A.
V. MODEL APPLYING

A. Equations model applied on the buck converter

In this work, we are not interested to the harmonic source $I_h$, expressed in (8) and represented in the Fig.7.

Actually, $Y_{LG}$ and $Y_{NG}$, expressed in (2) and appearing in the model of (8), are parasitical capacitances’ impedances to the referential conductor “G” [3]; they are expressed, respectively in (11) and (12).

The measurement is done by an experimental test using the impedance analyser 4294A. They are not dependent on the switching phenomena [3, 11].

Note that, in (11) and (12) impedances are an addition of two terms. The first one, is dependent on the inner capacitance $C_{LG}$ (or $C_{NG}$), the second term at $(1-\alpha)$ time, there is an addition capacitances ($C_m$ of the middle point “M”) which comes to be added on this inner capacitance. Moreover, the capacitance $C_m$ is added alternately, sometimes to the capacitance $C_{LG}$ sometime to $C_{NG}$.

$Y_{LN}$ expressed in (13), is the switching impedance, depending on: devices switching, the input capacitor impedance and the load impedance [3]. Neither $C_{NG}$ nor $C_{LG}$ are included in the $Y_{LN}$ expression.

\[
\begin{align*}
Y_{LG} &= \frac{\alpha}{l_p 2\pi f \cdot i} + \frac{1}{C_{LG} 2\pi f \cdot i} + \frac{1}{2\pi f \cdot i + \left(\frac{1}{\left(C_{LG} + C_m\right) 2\pi f \cdot i}\right)} \quad (11) \\
Y_{NG} &= \frac{1-\alpha}{l_p 2\pi f \cdot i} + \frac{\alpha}{C_{NG} 2\pi f \cdot i} + \frac{1}{2\pi f \cdot i + \left(\frac{1}{\left(C_{NG} + C_m\right) 2\pi f \cdot i}\right)} \quad (12) \\
Y_{LN} &= \left\{\frac{1}{Z_{CY}} + \frac{\alpha^2}{Z_f}\right\} + \left[\frac{\alpha^2}{Z_f} \sum_{m=1}^{\infty} \frac{\left(\sin(\pi m\alpha)\right)^2}{Z_f\left(f + mF_{sw}\right)}\right] \quad (13)
\end{align*}
\]

As a result, the DM impedance of the buck converter is depicted in the Fig.15, for different operation points, depending on the duty cycle $\alpha$. The result is compared to the decoupling capacitor impedance “$Z_{D}$” measured by the impedance analyser 4294A (yellow colour), and its serial element synthesised model (in black colour).

Note that this impedance matches with the input capacitor impedance in yellow colour all along a large frequency band, until 100MHz.

This result is helpful to identify DC-converters especially at the design stage.

According to (2), the DM impedance at low frequencies, trend to be as expressed bellow:

\[
Z_{DM} \approx \frac{Z_c(f)}{\alpha^2} = \frac{Z_c(f) + K_n}{Z_c(f) + Z_{boost}(f) - K_n} \quad (14)
\]

For a consequence, at low frequencies under 100Hz (this limit depends actually on converter’s components), the DM converter’s impedance (red and blue colour), depends on the output load impedance $Z_L$, and varies with the variation of the duty cycle $\alpha$ ($\alpha=0.3, 0.5, 0.8$). In other words, it depends on converter’s operation points.

The resonance appeared around 100MHz, is due to the interaction between $esl$ of the input capacitor $C_f$ and the parasitical line impedances $Z_p$. This will be detailed in the next section. After that frequency, the DM impedance takes the value of parasitical line impedance $Z_{l_p}$.

B. Model applied on the boost converter

The previous model is also applied on one more system which is a boost converter, in order to make a comparison and may be extract a general rule about the EMC converter identification.

The same analytical process is performed in this case, and is expressed on (15). Where:

- $Z_{boost}$ is the boost inductor impedance,
- $Z_{CY}$ is the input capacitor impedance,
- $Z_L$ is the load impedance,
- $Z_{lp}$ is the layout parasitical inductance,
- $Z_{CO}$ is the output capacitor impedance,

\[
Z_{DM} = Z_{CY}(f) + Z_{boost}(f) + K_n + Z_{l_p}(f) - K_n
\]

\[
K_n = (1-\alpha)^2 \sum_{n=0}^{\infty} \frac{Z_l(f-nF_{sw})}{Z_{CO}(f-nF_{sw})} \sin^2(\pi n(1-\alpha))
\]
The DM impedance of the boost converter is depicted in the Fig. 16 for three duty cycle (α=0.3, 0.5, 0.8) and compared to the input filter impedance.

It is important to outline that the DM converter’s impedance matches also here with the input filter impedance Z_{Cf} (red colour) along the frequency band of interest (150 kHz to 30MHz). Some distinctions appear due to resonances with the boost inductor around 1.5 kHz. Note that, at low frequencies (less than 100Hz), the impedance depends also on the duty cycle α, as outlined in the buck converter case.

Fig. 16. Impedance Z_{MD} of the boost converter

As showed in the Fig.15 and Fig.16, both spectrums of DM impedances of the buck or the boost converter give the impression that they are different –more resonances in the boost.

However, in a major way it’s necessary to point out that both impedances are matching the impedance of the input decoupling capacitors Z_{Cf} (red colour), all along a large frequency band. In other words, the differential mode impedance Y_{MD} of the buck or the boost converter is the same.

As a consequence, the knowledge of the converter impedance, which is connected directly to the EMC filter, can significantly enhance its optimisation and therefore reduce the EMC security margin.

VI. THE EFFECT OF SOME INTRINSIC PARAMETERS

In this section we will study the effect of some parameters of the buck converter on its DM impedance profile. Equations (2) and (11-13), reveal that for the buck converter case, the impedance model depends on some intrinsic converter’s parameters:

- The input capacitor value “C_{f}”
- The “esl” of the input capacitor “C_{f}”
- Parasitical capacitances to the ground C_{LG}, C_{NG} and C_{m}
- Parasitical capacitances on power devices sides: the Mosfet capacitance C_{ds} (between the drain and the source), the diode capacitance C_{diode}.

Those parameters have an actual effect on the impedance profile evolution in the spectral domain.

A. The effect of the input capacitor C_{f}

According to (2) and (11-13), the DM impedance depends on the Z_{Cf} impedance, otherwise on the value of the capacitor C_{f}.

Two profiles of the DM impedance associated to two input capacitors’ value are represented and compared on the Fig.17.

Note that there is an obvious difference between the two profiles. For the blue case (C_{f} = 10\mu F), the shape of the DM impedance seen at low frequencies, as expressed in (14) is extended until 300Hz, than that recorded for the red case (C_{f} = 100\mu F).

B. The effect of the esl of the capacitor C_{f}

For the same reason, the serial inductor element of the input capacitor “esl” has a major impact on the DM impedance profile especially at high frequencies. This is clearly visible on the Fig.18, between the blue and the red profiles, around the band of [1MHz, 100MHz].

Fig. 17. The comparison between two DM impedances profile about two values of the input capacitors C_{f}={10\mu F, 100\mu F}.

Fig. 18. The comparison between two DM impedances profile about two values of the “esl = {10nH, 50nH}” of the input capacitors C_{f}.
C. The effect of parasitical capacitances

Parasitical capacitances are the essential coupling path, supporting the CM current generated by converters, and throwing to the ground [10].

In this paper, the parasitical capacitances accounted are:
- \( C_{LG} \) the mutual parasitical capacitances seen between the “line” wire and the referential plane,
- \( C_{NG} \) the mutual parasitical capacitances seen between the “Neutral” wire and the referential plane,
- and \( C_m \) the mutual parasitical capacitances seen between the “middle point” of the switching cell and the referential plane.

The Fig.19 shows two DM impedance profiles for two parasitical capacitances values. Those values introduced in the model of the DM impedance expressed in (2) are comparatively exaggerated in order to make strongly in evidence the actual effect.

Note that, there is an impact in the impedance profile, appeared as resonances around 60MHz.

D. The effect of capacitances of the switching devices

Switching devices of the buck converter, studied in this paper (Fig.8), are Diode and Mosfet. Those devices are coupled to parallel capacitances.

Two profile cases are considered for two values of the Mosfet capacitances (\( C_d = 50 \text{pF} \) and \( 100 \text{pF} \)). The result is given in Fig.20 and Fig.21.

Note that, there is a significant difference between two impedances \( Y_{MD} \) deduced by two capacitances’ values, around 10MHz.

VII. CONCLUSIONS

In this paper we have presented a synthesis of input impedances of two dc-dc converters’ structures. Results point out that, the differential mode input impedance are matching along a large frequency band and are identical to the input decoupling capacitor. This result is helpful for filter optimisation.

In addition, we have presented some parameters impact on this impedance, such as the parasitical capacitances of the switching devices, the \( \text{esl} \) of the input capacitor and the parasitical capacitances to the ground.

The effect of each parameter appears and impact on the DM impedance profile.

Fig. 19. The comparison between two DM impedances profile for two values of parasitical capacitances.

Fig. 20. \( Y_{MD} \) impedance for two capacitances value of the Mosfet.

Fig. 21. Zoom of \( Y_{MD} \) impedance in the impact frequency zone.

REFERENCES


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