Analytical Models Synthesis of Power Electronic Converters

A. Ales, M.A. Cheurfi Belhadj, J-L. Schanen, D. Moussaoui, J. Roudet

***Abstract*—In this paper we proposes a synthesis of different mathematical models of power electronic converters based on *Thevenin*/*Norton* equivalent circuits. Those models, composed by impedances and harmonic noise sources, are helpful to predict the conducted ElectroMagnetic Interferences (EMI) generated by converters connected to the electrical network. Moreover, the extracted impedances are determining for sizing EMC filters. The proposed analytical model is tested with *PSpice* simulations and validated by experimental measurements, from DC frequency until 30MHz.**

***Index Terms*—EMC modeling, differential mode, common mode, EMC filter, LISN, EMI, conducted noise, noise source.**

I. INTRODUCTION

Nowadays, modern networks -such as the car's network supplying many electrical actuators- include many converters to manage efficiently the power transfer, which creates new issues and therefore the EMC study becomes more and more complex.

Generally, in modern embedded networks, integrated actuators are supplied by DC power, the reason that DC-converters are strongly needed, to manage the corresponding energy. For example, the input power at aeroplane turbine sides may be 10 times greater than at actuator sides. The velocity and position control need also the control of the input power.

In order to comply with ElectroMagnetic (EMC) standards, an accurate prediction of a common mode (CM) and differential mode (DM) conducted noise is necessary. Furthermore, since ElectroMagnetic Interference (EMI) filters are coupled to converters, the optimisation is necessary reached with the knowledge of converter's impedances [1–3].Several papers treat the converter's modelling with different techniques: Terminated/Unterminated models [4–6], lumped circuits [7–10]...etc. However, the proposed models deal only with one kind of converter, this cannot be generalised to other conditions, due to the parameter's dependency. This paper, presents a noise source analytical models of two converter's topologies, in order to highlight the impact of some parameters in the spectrum model profile, and highlights factors which actually make difference between such or that models.

This paper is organised in five sections. Section II gives the analytical computing process of the model. Section III is the application of the model on two converter structures. In the section IV we expose the impact of some parameters on the impedance. The last section concludes this paper.

II. GENERAL PURPOSE

DC-converters under some operation conditions are *Linear* and *Time Invariant* Systems (LTI), as mentioned in [2]. Based on this affirmation, they may be modelled by an equivalent Norton/Thevenin circuit. Moreover, converters under study are checked for this characteristic as demonstrated on the Fig.1. For frequencies higher than some tens of kHz, the input impedance is the same whatever the switches states.

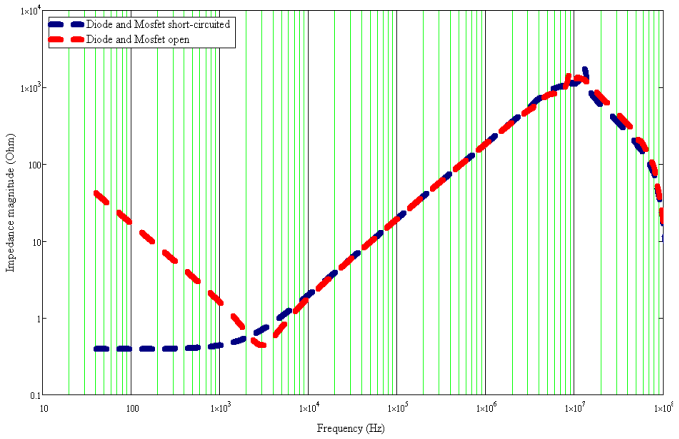


Fig. 1. Input DM impedance of a buck converter for two extreme case of switch state [2].

A. Converter impedances computing

The main purpose of this work is to make a study about DM converters' impedances taking into account its global behavior, such as the switching operation and PCB imperfections, and then extract a general law about a propagating path of DM conducted noise, by making a comparison point.

Power converters, especially DC-converters are supplied by two wires "L" for "*Plus*" and "N" for "*Minus*", but also connected to a third wire "*G*" which is the safety conductor commonly called "*Ground*" conductor, since the converter is the main source of conducted interferences, due to its operation principle. Thus, DC-converters may be considered as three ports systems, as drawn in the Fig.2 [11].Where: Z_{LG},

Z_{NG}, and Z_{LN} are respectively impedances supposed between two conductors *L*-*G*, N-G and L-N.

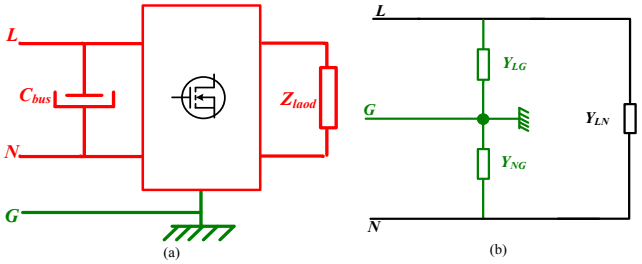


Fig. 2. Converter circuit topology: (a) converter circuit designed as an active multi-port circuit, (b) The equivalent π-quadripole circuit

In addition, by definition both CM impedance Z_{CM} and DM impedance Z_{DM} are computed according to the equation (1) [1] and [12].

Where I_{DM} is the current circulating between the two conductors "*L*" and "*N*", V_{DM} is the voltage between the same conductors. I_{CM} is the current circulating between the two previous wires including the safety conductor "*G*", V_{CM} is half the sum of the L-G and N-G voltages (Fig.2.a).

$$\begin{cases} Z_{DM} = \dfrac{V_{DM}}{I_{DM}} \\ Z_{CM} = \dfrac{V_{CM}}{I_{CM}} \end{cases} \quad (1)$$

According to the equation (1) and the circuit's topology of the Fig.2.b, the DM admittance Y_{DM} becomes as expressed in (2). Note that, this impedance depends, not only on the impedance "Z_{LN}" defined between the two wires L-N (which defines the DM concept), but also on impedances connected to the ground wire "G", Z_{LG} and Z_{NG} which are commonly supporting the CM current.

$$Y_{DM} = Y_{LN} + \left(\frac{Y_{LG} + Y_{NG}}{4}\right) \quad (2)$$

B. *The context of the study*

The main idea of this paper is to extract a reliable analytical model to compute the DM impedance of DC-converters topology, connected to an electrical network (Fig.3), on a frequency range from very low frequencies up to few tens of MHz.

The purpose in computing this impedance is multiple:

- To compute network impedance,
- To manage to make an EMC analysis of a whole network,
- To contribute on the EMI filter optimization,
- To enhance the converter design.

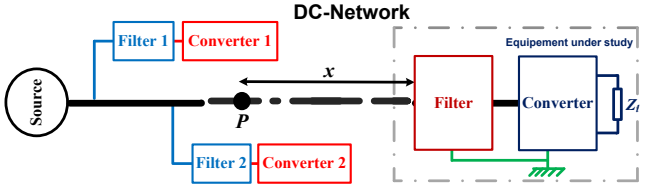


Fig. 3. Synoptic diagram of a DC-Network

III. ANALYTICAL MODELLING

A. *The switching function*

Any input signal $S_{in}(t)$ crossing throw any switching cell, as drawn in the Fig.4, is chopped according to the control law $sw(t)$ of the switching cell. The system outputs may be expressed according to (3).

$$S_{out}(t) = sw(t) \cdot S_{in}(t) \quad (3)$$

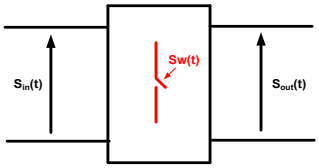


Fig. 4. Input and output signals crossing the system including the switching function $sw(t)$

The switching operator $sw(t)$, which is a T_{sw}-periodical function, actually establishes the switching law of the converter's devices and depends on the control strategy, which in this case concerns the buck and the boost converters' control, considering the duty cycle**"α"**.

Since the function $sw(t)$ corresponds to the switching signals, we can imagine that its shape in the temporal domain, is a "*one*" and "zero" sequence level as drawn in the Fig.5. According to the signal processing theory, the switching operator may be expressed as in (4), by the convolution between two conventional functions**,** [1-3] and [11]:

- $\Pi_{\alpha\frac{T_{sw}}{2}}(t)$ is the window function,
- $\text{III}_{T_{sw}}(t)$ is the Dirac Comb,
- Where T_{sw}=F_{sw}^{-1} is the switching period.
- α duty cycle,

$$sw(t) = \left(\Pi_{\alpha T_{sw}/2}\left(t - \frac{\alpha T_{sw}}{2}\right) \otimes \text{III}_{T_{sw}}(t)\right) \quad (4)$$

In the frequency domain, and by developing the convolution product, the output signal $S_{out}(f)$ (Fig.4) can be expressed as in (5), where F_{sw} is the switching frequency.

In fact, the $S_{out}(f)$ signal may be the converter current or voltage chopped at F_{sw} frequency whose importance will be highlighted when developing the expression.

$$S_{out}(f) = \alpha \sum_{k=-\infty}^{+\infty} \text{sinc}(\pi\alpha k) \cdot e^{-j2\pi\frac{\alpha k}{2}} \cdot S_{in}(f - kF_{sw}) \quad (5)$$

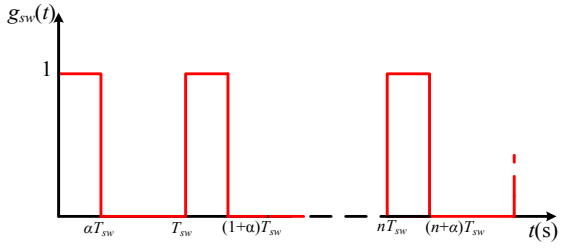


Fig. 5. The switching function.

B. *The modelling process*

As claimed previously, any three ports' converter (Fig.2.a) may be represented by an electrical circuit as depicted in the Fig.6 [11]. Z_{LISN} is the impedance of the *Line Impedance Stabilisation Network* "*LISN*".

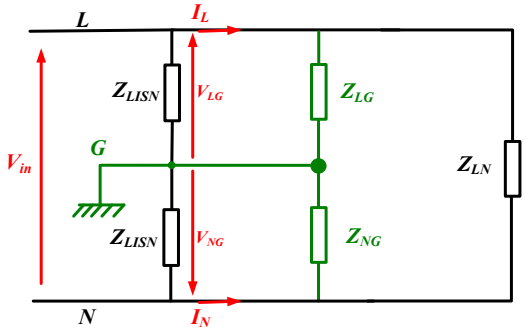


Fig. 6. A three ports converter model.

The input voltage V_{in} between wires "*L*" and "*N*", is in fact the DM voltage as expressed in (6). The DM current I_{DM} is expressed in (7).

$$V_{in} = V_{DM} = 0.5 * (V_{LG} - V_{NG}) \tag{6}$$

$$I_{MD}(f) = \frac{I_L - I_N}{2} \tag{7}$$

Since DC-converters, especially under study, are "*LTI*" systems as checked in the previous section, any multiport system may be formatted as an equivalent "*Norton*" (or *Thevenin*) circuit, regarded between two considered wires, such drawn in the Fig.7 [11] and [13].

For a consequence, the DM current related to the DM voltage may be expressed in (8). Where I_h regroup the noise current source, generated when the converter's operation. Y_{MD} is the converter's DM admittance [3].

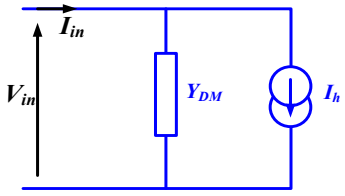


Fig. 7. Converter's models.

$$I_{MD}(f) = \frac{I_L - I_N}{2} = Y_{MD} \cdot V_{MD}(f) + I_h \tag{8}$$

IV. Converters under study

A. *Converters' topologies*

The DC-DC converters under study are schematised on Fig.8 and Fig.9. All essential coupling paths are introduced in order to be more accurate as in experiment, such as parasitical capacitances to the ground (C_{LG}, C_{NG}, and C_m for both the buck and the boost converter), parasitical line inductances l_p, parasitical elements of the boost inductor and imperfections of both capacitors C_f and C_o. [10].

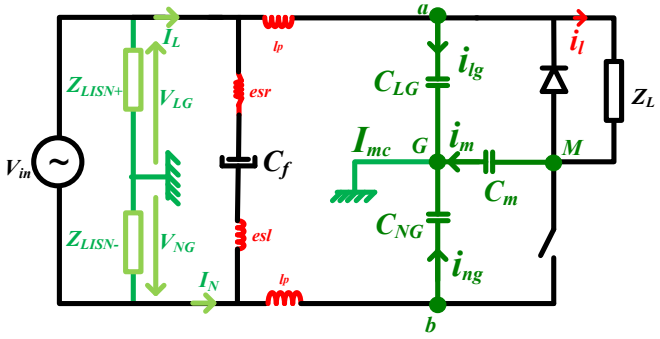


Fig. 8. The buck converterunder study.

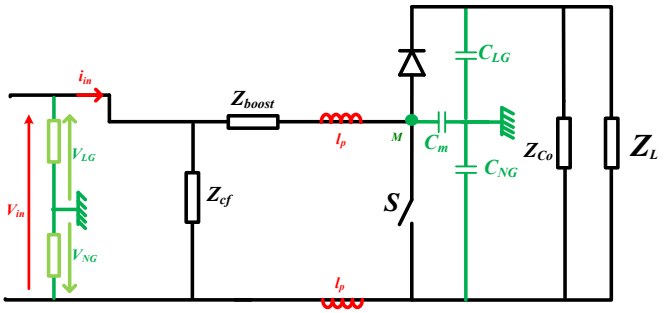


Fig. 9. The boost converter under study.

B. *Systems identification*

The identification, of different parameters of converters' topologies, drawn in Fig.8 and Fig.9, is performed by the impedance analyser "Agilent 4294A". The measurement setup is illustrated in Fig.10.

Fig. 10. The identification of converters' parameters.

1) Capacitors' model identification

The decoupling capacitor's impedance Z_{Cx} (C_x for C_f or C_o), is modelled by three serial elements: the *capacitance* "C_x", the *serial inductive element "esl"*, and the *serial resistive element "esr"* as expressed in (9). Those elements are identified by the impedance analyser 4294A. Fig.11 shows the comparison between the model and the measured impedance.

$$Z_{Cx}(P) = \frac{1}{C_x \cdot p} + esl \cdot p + esr \tag{9}$$

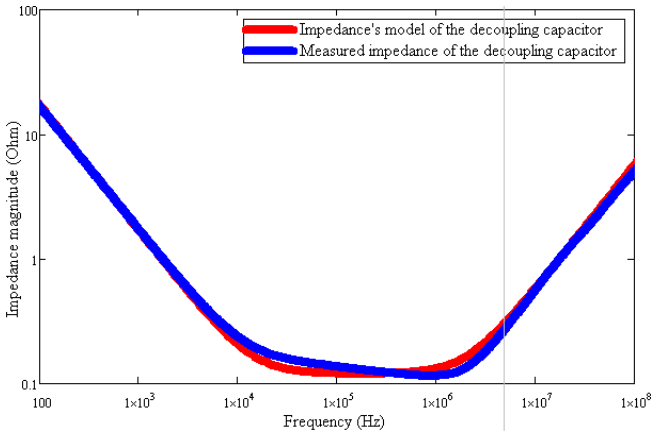


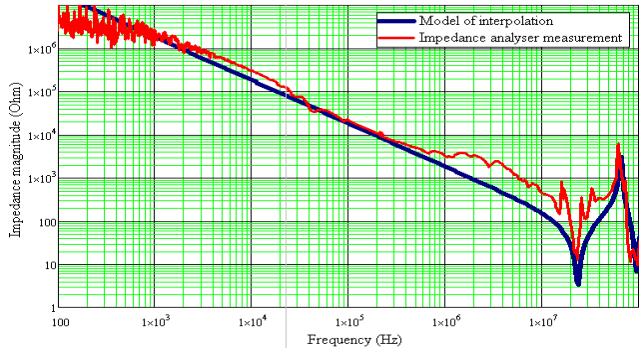
Fig. 11. The input capacitor's impedance: (red) the serial element model,(blue) the measured impedance.

2) Parasitical elements

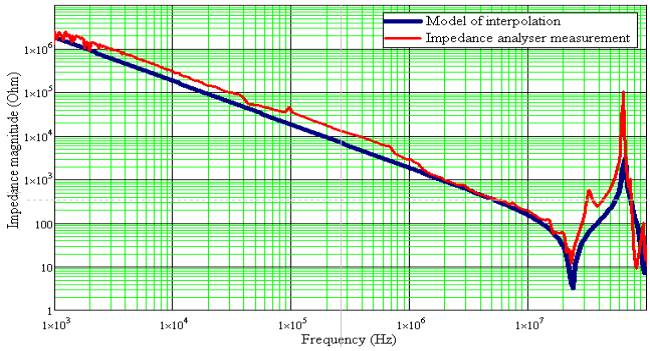
Converters' parasitical elements are identified by the impedance analyser 4294A. The parasitical elements such as, the line inductances l_p, the capacitances to the ground C_{LG}, C_{NG} and C_m, are deduced from measured impedances of the Fig.12, depicted between the "*L*" (or "*N*") and the "*G*" wire. The C_m capacitance, between the heatsink and the ground, is estimated according to (10), which is the plane capacitor equation.

$$C_m = \varepsilon_0 \varepsilon_r \frac{s}{e} \tag{10}$$

- ε_0 and ε_r are respectively the permittivity of the air and the relative permittivity of the insulator mica (ε_r=5)
- Z_{LG}: impedance between *Plus-Ground* wires,
- Z_{NG}: impedance between *Minus-Ground* wires,



(a)



(b)

Fig. 12. Impedances of the quadripolar model of the Fig.6: (a) Z_{LG} impedance between *Plus-Ground* wires, (b) Z_{NG}impedance between *Minus-Ground* wires.

3) Boost inductor

The boost inductor is the essential element in the Boost converter structure, since it is one which controls the variation of the current (state variable). Hence, its impedance is not without effect on the global DM impedance of the converter. Moreover, the equivalent HF model given in the Fig.13 is composed by a *parallel resistive element* "*epr*" and a *parallel capacitive element* "*ecp*".

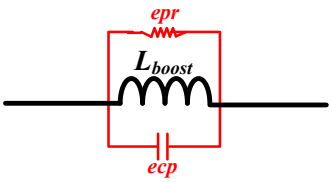


Fig. 13. The equivalent model of the boost inductor Z_{boost}

Fig.14 is the boost inductor impedance measured by the impedance analyser Agilent 4294A.

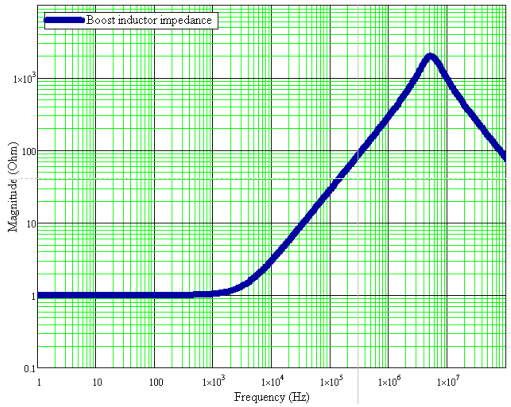


Fig. 14. Identification of the boost inductor impedance

V. MODEL APPLYING

A. Equations model applied on the buck converter

In this work, we are not interested to the harmonic source I_h, expressed in (8) and represented in the Fig.7.

Actually, Y_{LG} and Y_{NG}, expressed in (2) and appearing in the model of (8), are parasitical capacitances' impedances to the referential conductor "*G*" [3]; they are expressed, respectively in (11) and (12).

The measurement is done by an experimental test using the impedance analyser 4294A. They are not dependent on the switching phenomena [3, 11].

Note that, in (11) and (12) impedances are an addition of two terms. The first one, is dependent on the inner capacitance C_{LG} (or C_{NG}), the second term at (1-α) time, there is an addition capacitances (C_m of the middle point "*M*") which comes to be added on this inner capacitance. Moreover, the capacitance C_m is added alternately, sometimes to the capacitance C_{LG} sometimes to C_{NG}.

Y_{LN} expressed in (13), is the switching impedance, depending on: devices switching, the input capacitor impedance and the load impedance [3]. Neither C_{NG} nor C_{LG} are included in the Y_{LN} expression.

$$Y_{LG} = \frac{\alpha}{l_p 2\pi f \cdot i + \frac{1}{C_{LG} 2\pi f \cdot i}} + \frac{1-\alpha}{2\pi l_p f \cdot i + \left(\frac{1}{(C_{LG}+C_m)2\pi f \cdot i}\right)} \quad (11)$$

$$Y_{NG} = \frac{1-\alpha}{l_p 2\pi f \cdot i + \frac{1}{C_{NG} 2\pi f \cdot i}} + \frac{\alpha}{2\pi l_p f \cdot i + \left(\frac{1}{(C_{NG}+C_m)2\pi f \cdot i}\right)} \quad (12)$$

$$Y_{LN} = \left(\frac{1}{Z_{Cf}} + \frac{\alpha^2}{Z_l}\right) + \left[\alpha^2 \sum_{m=-\infty}^{+\infty} \left(\frac{(\mathrm{sinc}(\pi\alpha m))^2}{Z_l(f+mF_{sw})}\right)\right] \quad (13)$$

As a result, the DM impedance of the buck converter is depicted in the Fig.15, for different operation points, depending on the duty cycle *α*. The result is compared to the decoupling capacitor impedance "Z_{Cf}" measured by the impedance analyser 4294A (yellow colour), and its serial element synthesised model (in black colour).

Note that this impedance matches with the input capacitor impedance in yellow colour all along a large frequency band, until 100MHz.

This result is helpful to identify DC-converters especially at the design stage.

According to (2), the DM impedance at low frequencies, trend to be as expressed bellow:

$$Z_{DM} \approx \frac{Z_l(f)}{\alpha^2} \quad (14)$$

For a consequence, at low frequencies under 100Hz (this limit depends actually on converter's components), the DM converter's impedance (red and blue colour), depends on the output load impedance Z_l, and varies with the variation of the duty cycle *α* (*α*=0.3, 0.5, 0.8). In other words, it depends on converter's operation points.

The resonance appeared around 100MHz, is due to the interaction between *esl* of the input capacitor C_f and the parasitical line impedances l_p. This will be detailed in the next section. After that frequency, the DM impedance takes the value of parasitical line impedance Z_{lp}.

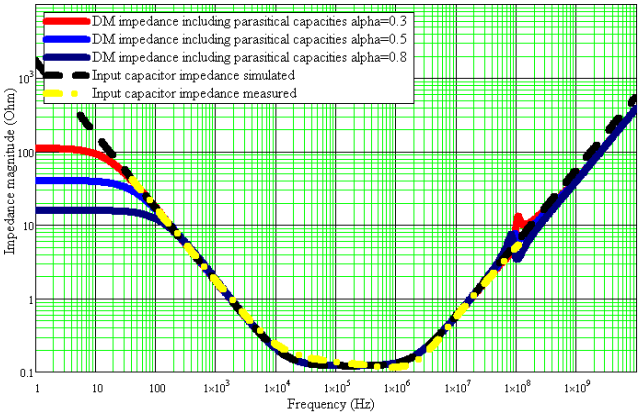


Fig. 15. The DM Impedance of the buck converter.

B. Model applied on the boost converter

The previous model is also applied on one more system which is a boost converter, in order to make a comparison and may be extract a general rule about the EMC converter identification.

The same analytical process is performed in this case, and is expressed on (15). Where:

- Z_{boost} is the boost inductor impedance,
- Z_{Cf} is the input capacitor impedance,
- Z_L is the load impedance,
- Z_{lp} is the layout parasitical inductance,
- Z_{C0} is the output capacitor impedance,

$$Z_{DM} = Z_{cf}(f)\frac{Z_{boost}(f)+K_n}{Z_{cf}(f)+Z_{boost}(f)-K_n} \quad (15)$$

$$K_n = (1-\alpha)^2 \sum_{n=0}^{\infty} (Z_l(f-nF_{sw}) // Z_{C0}(f-nF_{sw}))\sin c^2(\pi n(1-\alpha)) \quad (16)$$

The DM impedance of the boost converter is depicted in the Fig.16 for three duty cycle (α=0.3, 0.5, 0.8) and compared to the input filter impedance.

It is important to outline that the DM converter's impedance matches also here with the input filter impedance Z_{Cf}, (red colour) along the frequency band of interest (150 kHz to 30MHz). Some distinctions appear due to resonances with the boost inductor around 1.5 kHz. Note that, at low frequencies (less than 100Hz) the impedance depends also on the duty cycle α, as outlined in the buck converter case.

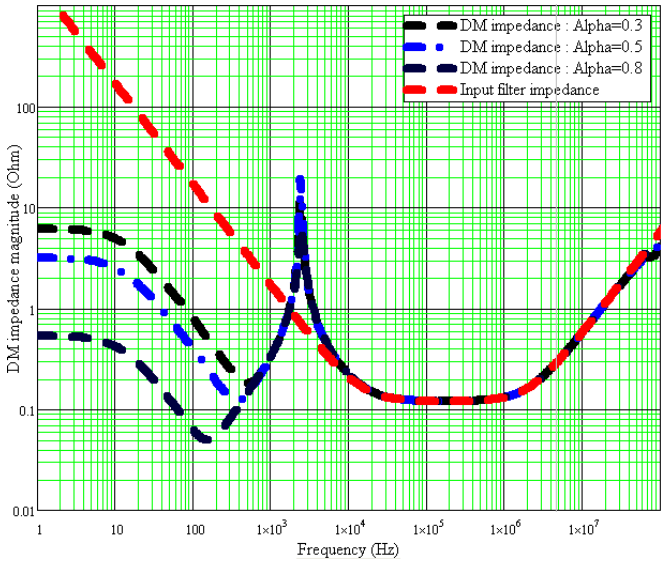


Fig. 16. Impedance Z_{MD} of the the boost converter

As showed in the Fig.15 and Fig.16, both spectrums of DM impedances of the buck or the boost converter give the impression that they are different –more resonances in the boost.

However, in a major way it's necessary to point out that both impedances are matching the impedance of the input decoupling capacitors Z_{Cf} (red colour), all along a large frequency band. In other words, the differential mode impedance Y_{MD} of the buck or the boost converter is the same.

As a consequence, the knowledge of the converter impedance, which is connected directly to the EMC filter, can significantly enhance its optimisation and therefore reduce the EMC security margin.

VI. THE EFFECT OF SOME INTRINSIC PARAMETERS

In this section we will study the effect of some parameters of the buck converter on its DM impedance profile. Equations (2) and (11–13), reveal that for the buck converter case, the impedance model depends on some intrinsic converter's parameters:

- The input capacitor value "C_f",
- The "*esl*" of the input capacitor "C_f",
- Parasitical capacitances to the ground C_{LG}, C_{NG} and C_m,
- Parasitical capacitances on power devices sides: the *Mosfet* capacitance C_{ds} (between the drain and the source), the diode capacitance C_{diode}.
- Parasitical line inductances l_p,

Those parameters have an actual effect on the impedance profile evolution in the spectral domain.

A. *The effect of the input capacitor C_f*

According to (2) and (11–13), the DM impedance depends on the Z_{Cf} impedance, otherwise on the value of the capacitor C_f.

Two profiles of the DM impedance associated to two input capacitors' value are represented and compared on the Fig.17.

Note that there is an obvious difference between the two profiles. For the blue case (C_f = 10µF), the shape of the DM impedance seen at low frequencies, as expressed in (14) is extended until 300Hz, than that recorded for the red case (C_f = 100µF).

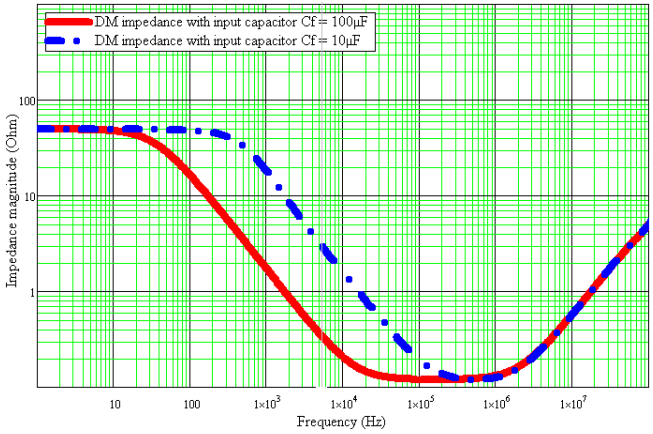


Fig. 17. The comparison between two DM impedances profile about two values of the input capacitors C_f={10µF, 100µF}.

B. *The effect of the esl of the capacitor C_f*

For the same reason, the serial inductor element of the input capacitor "*esl*" has a major impact on the DM impedance profile especially at high frequencies. This is clearly visible on the Fig.18, between the blue and the red profiles, around the band of [1MHz, 100MHz].

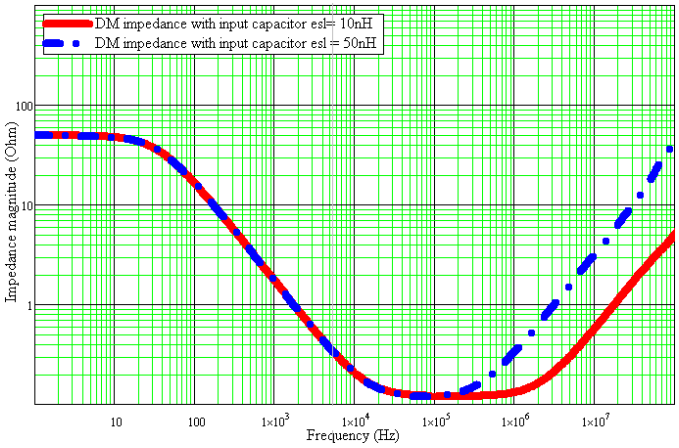


Fig. 18. The comparison between two DM impedances profile about two values of the "*esl* = {10nH, 50nH}" of the input capacitors C_f.

C. *The effect of parasitical capacitances*

Parasitical capacitances are the essential coupling path, supporting the CM current generated by converters, and throwing to the ground [10].

In this paper, the parasitical capacitances accounted are:

- C_{LG} the mutual parasitical capacitances seen between the "*line*" wire and the referential plane,
- C_{NG} the mutual parasitical capacitances seen between the "*Neutral*" wire and the referential plane,
- and C_m the mutual parasitical capacitances seen between the "*middle point*" of the switching cell and the referential plane,

The Fig.19 shows two DM impedance profiles for two parasitical capacitances values. Those values introduced in the model of the DM impedance expressed in (2) are comparatively exaggerated in order to make strongly in evidence the actual effect.

Note that, there is an impact in the impedance profile, appeared as resonances around 60MHz.

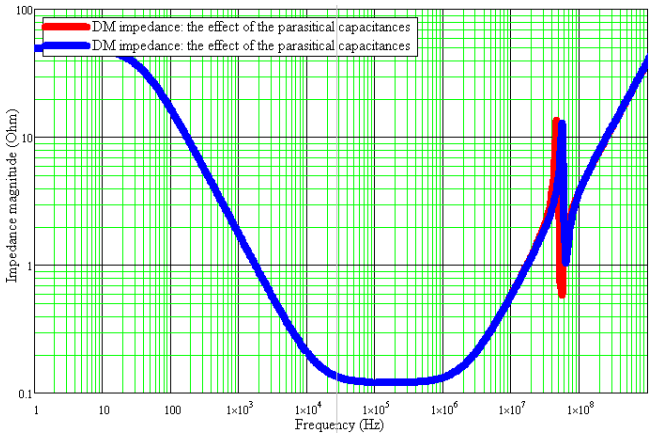


Fig. 19. The comparison between two DM impedances profile for two values of parasitical capacitances.

D. *The effect of capacitances of the switching devices*

Switching devices of the buck converter, studied in this paper (Fig.8), are *Diode* and *Mosfet*. Those devices are coupled to parallel capacitances.

Two profile cases are considered for two values of the *Mosfet* capacitances (C_{ds}=50pF and 100pF). The result is given in Fig.20 and Fig.21.

Note that, there is a significant difference between two impedances Y_{MD} deduced by two capacitances' values, around 10MHz.

VII. CONCLUSIONS

In this paper we have presented a synthesis of input impedances of two dc-dc converters' structures. Results point out that, the differential mode input impedance are matching along a large frequency band and are identical to the input decoupling capacitor. This result is helpful for filter optimisation.

In addition, we have presented some parameters impact on this impedance, such as the parasitical capacitances of the switching devices, the *esl* of the input capacitor and the parasitical capacitances to the ground.

The effect of each parameter appears and impact on the DM impedance profile.

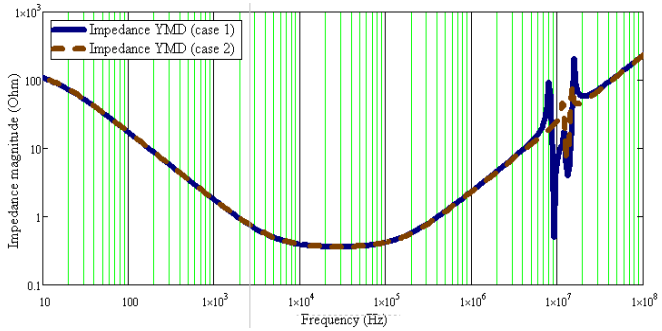


Fig. 20. Y_{MD} impedance for two capacitances value of the Mosfet

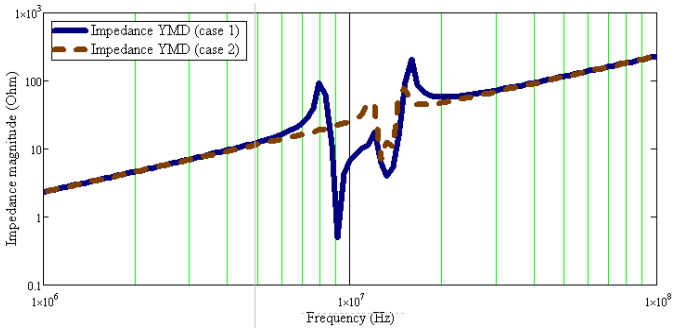


Fig. 21. Zoom of Y_{MD} impedance in the impact frequency zone

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Achour Ales received the diploma in electrical engineering from Ecole Militaire Polytechnique school, Algiers, Algeria in 2006. He obtained his Master in Electrical Engineering from Ecole Militaire Polytechnique school , Algiers, Algeria in 2009. He received His Ph.D at Grenoble University, Grenoble, France since 2015. His current research interest the Electromagnetic compatibility of the embedded network and power electronics.

Jean-Luc Schanen (M’99–SM’04) was born in 1968. He received the Electrical Engineering Diploma and Ph.D. degrees from Grenoble Institute of Technology, Grenoble, France, in 1990 and 1994, respectively. He is currently a Professor with Grenoble Institute of Technology. He has been with the Grenoble Electrical Engineering Laboratory, St. Martin d’Hères, France, since 1994, working in the field of power electronics. His main activities concern the technological design of power converters. His research team uses (or develops if not available) all kinds of modeling tools in order to improve the performance of power electronics converters, including electromagnetic compatibility and thermal aspects.
Prof. Schanen is a Senior Member of the IEEE Power Electronics Society and IEEE Industry Applications Society, and was Chairman of the Power Electronics Devices and Components Committee of the IEEE Industry Applications Society between 2006 and 2007.

Djelloul Moussaoui graduated in Electrical Engineering from Ecole Militaire Polytechnique d'Algiers, Algeria in 1987. He obtained his Ph.D in Electrical Engineering from Grenoble Institute of Technology, France in 1997. He became Professor in 2010, and is currently leading research in EMC in Power Electronics.

James Roudet was born in 1962. He holds PHD (1990) and electrical engineering diploma (1986). He is Professor at Grenoble University (Université Joseph Fourier, France), within the G2ELab (Grenoble Electrical Engineering Lab), in the field of power electronics. First research interest concerned resonant converters. Afterwards, he promoted EMC activities in the field of power electronics, and developed a leading activity in the technological design of power converters. He currently holds the director position of G2ELab, after several years of leading the power electronics team.